April 20, 2023

ASIC Design Engineer (Greece)

EdgeQ Greece ΜΟΝΟΠΡΟΣΩΠΗ ΙΔΙΩΤΙΚΗ ΚΕΦΑΛΑΙΟΥΧΙΚΗ ΕΤΑΙΡΕΙΑ
(EdgeQ Greece Single Member P.C)

ABOUT EDGEQ

EdgeQ is a leading innovator creating the industry's first 5G Base-Station-on-a-Chip. Led by seasoned executives from Qualcomm, Intel, and Broadcom who have delivered industry-transforming technologies (4G/5G, WiFi, Wimax, Artificial Intelligence, Cloud Servers) for the last few decades, EdgeQ is inventing a new paradigm in 5G wireless infrastructure. Our vision is to reconstitute wireless infrastructure into a fluid, cloud-based form that would extend robust internet access and communications to remote and dense areas, as well as to the next trillion of interconnected devices. EdgeQ is backed by world-renown investors, including Greece-based Phaistos Investment Fund, Threshold Ventures, AME Ventures, SDF - - the investment arm of the United Arab Emirates Tawazun Council, Singapore-based global investor EDBI, IRONGREY, ST Engineering, Yaletown, and ClearSky.

Role Summary & Responsibilities

- As a member of a world-class team that has delivered multiple generations of modems to all Android and Apple mobile phones, you will be working on the ASIC design of EdgeQ's next generation chip. You would be in the hardware systems team working on next Gen 5G Platform Architecture.
- Design the micro-Architecture of high performance and low power hardware from scratch. Work with architect and software teams.
- Design, simulation and synthesis for area/timing/power/performance specifications
- RTL implementation of wireless SoC and MAC modules from spec to tape out - Control and Datapath RTL development, Lint/CDC of RTL blocks and integration of subsystems.
- Design SoC and MAC architectures, including hardware accelerators, memory, I/Os, peripherals, and control interfaces
- Work in the front end SoC team with architects, designers and verification engineers and be responsible for the design and verification of Modem IPs and SoC.
- Work in the Physical Design Team on advanced Technology Nodes learning and owning PNR implementation (Floorplanning, Placement, CTS, post route, Timing Closure, IR Drop etc).
- RTL implementation of baseband processing modules from spec to tape out.

Job Requirements & Qualifications

- MS or PHD in Electrical Engineering.
- Experience in cellular wireless communications (4G/5G) a plus
- Knowledge / experience on SystemVerilog and C
- Knowledge on digital signal processing (e.g. Nyquist Sampling Theorem, LTI, Digital filter, Fourier transform, Z-transform, DFT/FFT, etc.)
- Familiar with RTL simulator, RTL synthesis tools, GCC, and Python
- Maximum Likelihood Decoder HW design experience
- Strong digital logic design skills using FSMs, Boolean logic, arithmetic logic a plus.

Check out our website: https://edgeq.io/!

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